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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/687,858	10/13/2000	Chak Cheung Edward Ho	0100.0000780	8827

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EXAMINER	
CHANG, ERIC	

ART UNIT	PAPER NUMBER
2116	5

DATE MAILED: 02/10/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/687,858	EDWARD HO ET AL.	
	Examiner	Art Unit	
	Eric Chang	2116	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *17 November 2003*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-6,8-11,13-16 and 18-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-6,8-11,13-16 and 18-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. §§ 119 and 120

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

13)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application) since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

a) ☐ The translation of the foreign language provisional application has been received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121 since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

1. Claims 1-6, 8-11, 13-16 and 18-20 are pending.

Claim Objections

2. Claims 19 are objected to because of the following informalities: There are two claims numbered 19; the first of which appears to be a duplicate of claim 1. Appropriate correction is required.

Response to Arguments

3. Applicant's arguments with respect to claims 1-6, 8-11, 13-16 and 18-20 have been considered but are moot in view of the new ground(s) of rejection.

Claim Rejections - 35 USC § 103

4. The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

5. Claims 1-2, 4, 6, 8-10, 13-15 and 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant's admitted prior art, in view of U.S. Patent 6,067,272 to Foss.

6. As to claim 1, in the Background of the Invention section of the Disclosure, Applicant discloses as prior art a signal phase shifting circuit to shift the phase of a STROBE signal, comprising:

[a] a reference signal period dividing circuit comprising a phase shift generator that receives a reference and a feedback control signal and outputs a delay control signal for a variable delay circuit [FIG. 1, element 22, and page 4, lines 1-14]; and

[b] a variable delay circuit to provide a phase shifted output of the STROBE signal based on the delay control signal from the reference signal period dividing circuit [FIG. 1, element 28, and col. 4, lines 16-22], and that output signal is associated with the STROBE signal [FIG. 1, element 12] of a double data rate communication [page 1, lines 27].

Applicant teaches all of the limitations in the claim exist in the admitted prior art, including use of a STROBE signal for double data rate communication, but does not teach that a feedback delay matching circuit is coupled to the output of the phase shift generating circuit to produce the feedback control signal.

Foss teaches that a feedback delay matching circuit representing a delay model [col. 3, lines 63-67, and col. 4, lines 1-6] may be used in the construction of a delay locked loop [col. 2, lines 48-55]. Specifically, Foss teaches that the feedback delay matching circuit is coupled to the output of the phase shifting circuit [FIG. 5, elements 29, 33 and 31] in order to produce the feedback control signal in order to compensate for variations in operating conditions [col. 4, lines 1-6]. Foss further teaches that the use of such a clock applying circuit, including the feedback delay matching circuit, can be used not only in SDRAMs, but also in other synchronous memories, such as a DDR SDRAM, substantially as claimed.

At the time that the invention was made, it would have been obvious to a person of ordinary skill in the art to employ feedback delay matching means as taught by Foss. One of

ordinary skill in the art would have been motivated to do so to reduce clock skew within a memory access system.

It would have been obvious to one of ordinary skill in the art to combine the teachings of the cited references because they are both directed to the problem of clocking a memory system. Moreover, the feedback delay matching means taught by Foss would improve the flexibility of admitted prior art because it allowed the memory to operate at high speeds and maintain its capability as operating conditions vary.

7. As to claims 2, 4, 10 and 15, Applicant discloses as prior art the variable delay circuit includes a delay stage and at least one phase shifted output signal drive buffer [FIG. 1, element 40, and page 4, lines 16-22]. Applicant also discloses as prior art the variable delay circuit includes a multiplexer coupled to the delay stage [FIG. 1, element 42].

8. As to claim 6, Applicant discloses as prior art discloses a data latch having a first input to receive data and a second input coupled to receive the phase shifted output signal [FIG. 1, element 16, and page 3, lines 24-31].

9. As to claims 8, 13 and 18, Applicant discloses as prior art discloses the phase shift generating circuit includes a plurality of serially coupled buffers forming a controlled delay stage [FIG. 1, element 37]. Furthermore, Foss discloses the feedback delay matching circuit includes a plurality of serially couple multiplexer and buffer stages coupled to the controlled delay stage [FIG. 5, elements 25 and 27, and col. 3, lines 36-45].

10. As to claim 9, Applicant discloses as prior art discloses a signal phase shifting circuit for use with a STROBE signal for double data rate communication, substantially as claimed. Furthermore, Applicant teaches that the phase shift generating circuit includes a DLL comprising a phase detection circuit, a charge pump, and a loop filter [FIG. 1, elements 30, 32, and 34, and page 4, lines 1-8].

11. As to claim 14, Applicant discloses as prior art discloses a signal phase shifting circuit for use with a STROBE signal for double data rate communication, substantially as claimed. Furthermore, Applicant teaches that the signal phase shifting circuit is used in a data receiving circuit [page 3, lines 24-31] that further comprises a data latch coupled to receive data and the phase-shifted output from the signal phase shifting circuit [FIG. 1, element 16].

12. Claims 3, 5, 11, 16, 19 and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant's admitted prior art, in view of U.S. Patent 6,067,272 to Foss, and in further view of U.S. Patent 5,878,055 to Allen.

13. As to claims 3, 5, 11 and 16, Foss discloses the feedback delay matching circuit uses similar elements as the clock delay path [col. 3, lines 63-67, and col. 4, line 1]. Foss teaches that the clock delay path includes a plurality of serially coupled buffer stages, or a plurality of multiplexer and buffer stages [FIG. 5, elements 25 and 27, and col. 3, lines 36-45], to compensate for delay variations [col. 4, lines 1-6]. Applicant and Foss teach all of the

limitations of the claim, and suggest the combination of components within the feedback delay matching circuit, but do not specifically teach that said feedback delay matching circuit comprises the serially coupled multiplexer and buffer stages.

As to claims 19 and 20, Allen teaches a programmable delay path comprising serially coupled multiplexer and buffer stages [FIG. 4, and col. 5, lines 19-67, and col. 6, lines 1-24], and that use of such a delay path is used to reduce clock skew, including skew introduced by variations in operating conditions [col. 1, lines 59-67].

At the time that the invention was made, it would have been obvious to a person of ordinary skill in the art to employ the serially coupled multiplexer and buffer stages in a delay as taught by Allen. One of ordinary skill in the art would have been motivated to do so that the feedback signal would be correctly delayed to properly shift the STROBE signal for double data rate communications, substantially as claimed.

It would have been obvious to one of ordinary skill in the art to combine the teachings of the cited references because they are both directed to the problem of correcting for clocking errors caused by variations in operating conditions. Moreover, the delay means taught by Allen would improve the implementation of Applicant and Foss because it allowed the specifics of the feedback delay matching circuit to be described in detail.

14. As to claims 19 and 20, Allen teaches that a number of methodologies are available for using the serially coupled multiplexer and buffer stages to achieve the proper delay setting [FIG. 5, elements 25 and 27, and col. 3, lines 36-45], thereby obtaining the desired resolution. Within such guidelines, it would therefore be obvious to one of ordinary skill in the art to have each

multiplexer and buffer stage control an equal fraction of the clock cycle. By doing so, the number of stages would be the reciprocal of the desired fraction of the clock cycle, substantially as claimed.

Conclusion

15. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

16. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Eric Chang whose telephone number is (703) 305-4612. The examiner can normally be reached on M-F 9:00-5:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Thomas Lee can be reached on (703) 305-9717. The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 305-3900.

ec
1/27/2004

THOMAS LEE
SUPERVISORY PATENT EXAMINER
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